



Switch Memory Architectures

With the widespread use of high performance embedded devices in "information appliances" such as cell phones, PDAs, and other hand-held devices, the electronic design industry is faced with the challenge of reducing the cost and design time of high-performance embedded systems.

The current invention, switch memory architectures (SMAs), is a class of parallel architectures intended for a direct silicon implementation in either electronic or optical systems. SMAs may be systematically derived and are suitable for a wide range of targets. Derivation and application-specific configuration of SMAs use a well-developed mathematical formalism called the polyhedral model, which permits the expression of compute intensive algorithmic kernels and systematic derivation of SMA tailored specific kernel.

SMAs are related to, but more powerful than, an earlier technology called systolic arrays. Systolic arrays are an n-dimensional, locally connected grid of simple processing elements (PEs) wherein each PE is pre-configured for a specific task and thus has no instruction overhead. Precise data-transfer and control between the PEs result in the parallel solution of the application. In contrast, SMAs are a grid of PEs connected through the ISWITCH that allows long connections that can be rapidly, easily and dynamically reconfigured. The reconfiguration, however, is restricted in scope and thus has a low cost. Nevertheless, they are necessary and sufficient for an efficient (optimal under certain constraints) regular implementation of the targeted applications.

In contrast to systolic arrays, in which the grid is usually one or two dimensional, SMAs reasonably have a minimum of three dimensions and are as a result particularly relevant for optical or 3D VLSI. The higher dimensionality is possible because SMAs relax the "locality-constraint" on the PEs of systolic architectures.

In summary, SMAs are a new architectural model intended for direct silicon implementation in either electronic or optical systems. On-chip memory may be used to store and transfer intermediate values, and reconfiguration may be used for run-time switching of the memory-processor interconnect. A device of the present invention may be suitable for a wide range of target technologies ranging from ASIC and FPGAs to more general reconfigurable computing platforms.

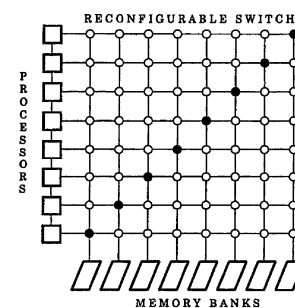
An online demo and further technical information (including publications) is available at: www.cs.colostate.edu/~svt/GRAIL/.

Please contact us for more information on licensing and partnering opportunities.

ID: CSURF 03-039

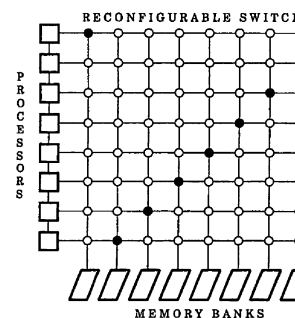
Patent Information
U.S. patent 7,412,586
(issued)

Inventor Information
Sanjay Rajopadhye
Gautam Gupta
Lakshminarayanan
Renganarayana



Features and Benefits

- Switch memory architectures (SMAs) are a new model of parallel architectures intended for direct silicon implementation in either electronic or optical systems, including 3D VLSI.
- SMAs relax the locality-constraint inherent to the systolic model, which they generalize and improve. They can be automatically derived from high-level program specifications.
- SMAs are suitable for a wide range of target technologies, from ASIC and FPGAs to more general reconfigurable computing platforms.



Contact Information:

Jeremy Nelson
Phone: 970.491.7100
Email: jeremy.nelson@colostate.edu
www.csurf.org/tto